UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/687,858	10/13/2000	Chak Cheung Edward Ho	0100.0000780	8827

7590 03/25/2005

Markison & Reckamp P C
P O Box 06229
Wacker Drive
Chicago, IL 60606-0229

EXAMINER	
CHANG, ERIC	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/687,858	EDWARD HO ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-11,13-16 and 18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,13-16 and 18-20* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6, 8-11, 13-16 and 18-21 are pending.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-2, 4, 6, 8-10, 13-15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, in view of U.S. Patent 6,067,272 to Foss.

4. As to claim 1, in the Background of the Invention section of the Disclosure, Applicant discloses as prior art a signal phase shifting circuit to shift the phase of a STROBE signal, comprising:

> [a] a reference signal period dividing circuit comprising a phase shift generator that receives a reference and a feedback control signal and outputs a delay control signal for a variable delay circuit [FIG. 1, element 22, and page 4, lines 1-14]; and
>
> [b] a variable delay circuit to provide a phase shifted output of the STROBE signal based on the delay control signal from the reference signal period dividing circuit [FIG. 1, element 28, and col. 4, lines 16-22], and that output signal is associated with the STROBE signal [FIG. 1, element 12] of a double data rate communication [page 1, lines 27].

Applicant teaches all of the limitations of the claim exist in the admitted prior art, including use of a STROBE signal for double data rate communication, but does not teach that a feedback delay matching circuit is coupled to the output of the phase shift generating circuit to produce the feedback control signal.

Foss teaches that a feedback delay matching circuit representing a delay model [col. 3, lines 63-67, and col. 4, lines 1-6] may be used in the construction of a delay locked loop [col. 2, lines 48-55]. Specifically, Foss teaches that the feedback delay matching circuit is coupled to the output of the phase shifting circuit [FIG. 5, elements 29, 33 and 31] in order to produce the feedback control signal in order to compensate for variations in operating conditions [col. 4, lines 1-6]. Foss further teaches that the use of such a clock applying circuit, including the feedback delay matching circuit, can be used not only in SDRAMs, but also in other synchronous memories, such as a DDR SDRAM, substantially as claimed. Thus, Foss teaches a delay locked loop to synchronize memory data with a clock input [col. 2, lines 43-50] by phase shifting the clock to reduce skew for accessing the memory [col. 2, lines 56-65] similar to that of the admitted prior art. Foss further teaches a delay model to compensate for delay variations [col. 4, lines 1-6].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ feedback delay matching means as taught by Foss to phase shift the STROBE signal of the admitted prior art. One of ordinary skill in the art would have been motivated to do so to reduce clock skew when accessing a synchronous dynamic memory.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of using a delay lock loop to

clock a memory system. Moreover, by applying the feedback delay matching means taught by Foss towards the delay lock loop to shift the phase of the STROBE signal of admitted prior art, the DDR memory would be able to operate at high speeds and maintain its capability even as operating conditions vary.

5. As to claims 2, 4, 10 and 15, Applicant discloses as prior art the variable delay circuit includes a delay stage and at least one phase shifted output signal drive buffer [FIG. 1, element 40, and page 4, lines 16-22]. Applicant also discloses as prior art the variable delay circuit includes a multiplexer coupled to the delay stage [FIG. 1, element 42].

6. As to claim 6, Applicant discloses as prior art discloses a data latch having a first input to receive data and a second input coupled to receive the phase shifted output signal [FIG. 1, element 16, and page 3, lines 24-31].

7. As to claims 8, 13 and 18, Applicant discloses as prior art discloses the phase shift generating circuit includes a plurality of serially coupled buffers forming a controlled delay stage [FIG. 1, element 37]. Furthermore, Foss discloses the feedback delay matching circuit includes a plurality of serially couple multiplexer and buffer stages coupled to the controlled delay stage [FIG. 5, elements 25 and 27, and col. 3, lines 36-45].

8. As to claim 9, Applicant discloses as prior art discloses a signal phase shifting circuit for use with a STROBE signal for double data rate communication, substantially as claimed.

Furthermore, Applicant teaches that the phase shift generating circuit includes a DLL comprising a phase detection circuit, a charge pump, and a loop filter [FIG. 1, elements 30, 32, and 34, and page 4, lines 1-8].

9. As to claim 14, Applicant discloses as prior art discloses a signal phase shifting circuit for use with a STROBE signal for double data rate communication, substantially as claimed. Furthermore, Applicant teaches that the signal phase shifting circuit is used in a data receiving circuit [page 3, lines 24-31] that further comprises a data latch coupled to receive data and the phase-shifted output from the signal phase shifting circuit [FIG. 1, element 16].

10. Claims 3, 5, 11, 16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, in view of U.S. Patent 6,067,272 to Foss, and in further view of U.S. Patent 5,878,055 to Allen.

11. As to claims 3, 5, 11 and 16, Foss discloses the feedback delay matching circuit uses similar elements as the clock delay path [col. 3, lines 63-67, and col. 4, line 1]. Foss teaches that the clock delay path includes a plurality of serially coupled buffer stages, or a plurality of multiplexer and buffer stages [FIG. 5, elements 25 and 27, and col. 3, lines 36-45], to compensate for delay variations [col. 4, lines 1-6]. Applicant and Foss teach all of the limitations of the claim, and suggest the combination of components within the feedback delay matching circuit, but do not specifically teach that said feedback delay matching circuit comprises the serially coupled multiplexer and buffer stages.

As to claims 19 and 20, Allen teaches a programmable delay path comprising serially coupled multiplexer and buffer stages [FIG. 4, and col. 5, lines 19-67, and col. 6, lines 1-24], and that use of such a delay path is used to reduce clock skew, including skew introduced by variations in operating conditions [col. 1, lines 59-67].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the serially coupled multiplexer and buffer stages in a delay as taught by Allen. One of ordinary skill in the art would have been motivated to do so that the feedback signal would be correctly delayed to properly shift the STROBE signal for double data rate communications, substantially as claimed.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of correcting for clocking errors caused by variations in operating conditions. Moreover, the delay means taught by Allen would improve the implementation of Applicant and Foss because it allowed the specifics of the feedback delay matching circuit to be described in detail.

12. As to claims 19 and 20, Allen teaches that a number of methodologies are available for using the serially coupled multiplexer and buffer stages to achieve the proper delay setting [FIG. 5, elements 25 and 27, and col. 3, lines 36-45], thereby obtaining the desired resolution. Within such guidelines, it would therefore be obvious to one of ordinary skill in the art to have each multiplexer and buffer stage control an equal fraction of the clock cycle. By doing so, the number of stages would be the reciprocal of the desired fraction of the clock cycle, substantially as claimed.

Allowable Subject Matter

13. Claim 21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

14. Applicant's arguments filed June 14, 2004 have been fully considered but they are not persuasive.

15. In the remarks, applicants argued in substance that Foss does not teach or suggest compensating a clock input and a STROBE input nor compensating for delay variations associated with a phase shifted output signal drive buffer located in a variable delay circuit that receives a STROBE signal. Specifically, applicants argue that although Foss teaches a delay to compensate for delays for an input clock signal, Foss does not teach how delays associated with a STROBE signal are compensated for.

16. But applicant's admitted prior art teaches means by which a STROBE signal is suitably delayed in order to enable proper DDR data transfer [page 3, lines 24-31], and in particular how to compensate for delay variations associated with a phase shifted output signal drive buffer located in a variable delay circuit that receives a STROBE signal [page 4, lines 16-26].

Furthermore, applicant specifically admits that such a delay control circuit comprises a DLL [page 4, lines 1-14].

17. Foss teaches means by which delays associated with a clock input are compensated for [col. 2, lines 56-65], wherein said means comprise a delay model [col. 3, lines 63-67, and col. 4, lines 1-6], substantially as claimed. Specifically, Foss teaches modifying a DLL in order to achieve said compensation [col. 2, lines 43-55].

18. Thus, applicant admits means to compensate for delay variations associated with a phase shifted output signal drive buffer located in a variable delay circuit that receives a STROBE signal using a DLL, and Foss teaches means for modifying a DLL in order to compensate for delays associated with a clock input. As applicants admit in the arguments, the DLL circuit of Foss is closely related to the clock signal period dividing DLL circuit 22 as known in the prior art.

19. Accordingly, it would have been obvious to one of ordinary skill in the art to combine the teachings of the applicant's admitted prior art and the teachings of Foss, because they are both directed to compensating for delay variations using means comprising a DLL. Furthermore, combining the admitted prior art with the teachings of Foss would compensate both a clock input and a STROBE input for delay variations associated with a phase shifted output signal drive buffer located in a variable delay circuit that receives a STROBE signal, substantially as claimed.

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 9, 2005
ec

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100